Міністерство освіти та науки України

Національний технічний університет України

**«Київський політехнічний інститут»**

Факультет прикладної математики

Кафедра спеціалізованих комп’ютерних систем

##### ЛАБОРАТОРНА РОБОТА №3

з дисципліни

«Технологія проектування комп’ютерних систем»

«*Побудова моделі синхронного тригера*»

**Виконав:**

Курс: 4

Група: КВ-92

Степанюк Михайло Федорович

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**Завдання**

1) Описати модель тригера використовуючи лише мову A-VHDL

2) Побудувати модель тригера, використовуючи моделі логічних елементів, створених в попередніх лабораторних роботах.

3) Побудувати часові діаграми роботи логічного елемента

**Варіант №15**

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2)Код на мові А-VHDL:

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entity and3 is*

*port (*

*in1: in STD\_LOGIC;*

*in2: in STD\_LOGIC;*

*in3: in STD\_LOGIC;*

*out1: out STD\_LOGIC*

*);*

*end and3;*

*--}} End of automatically maintained section*

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entity or2 is*

*port (*

*in1: in STD\_LOGIC;*

*in2: in STD\_LOGIC;*

*out1: out STD\_LOGIC*

*);*

*end or2;*

*--}} End of automatically maintained section*

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entity not3 is*

*port (*

*in1: in STD\_LOGIC;*

*in2: in STD\_LOGIC;*

*in3: in STD\_LOGIC;*

*out1: out STD\_LOGIC;*

*out2: out STD\_LOGIC;*

*out3: out STD\_LOGIC*

*);*

*end not3;*

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entitys\_comb is*

*port (*

*Q: in STD\_LOGIC;*

*FT: in STD\_LOGIC;*

*C: in STD\_LOGIC;*

*nQ: in STD\_LOGIC;*

*F1: out STD\_LOGIC;*

*F2: out STD\_LOGIC*

*);*

*ends\_comb;*

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entitys\_bistable is*

*port (*

*R: in STD\_LOGIC;*

*F1: in STD\_LOGIC;*

*F2: in STD\_LOGIC;*

*S: in STD\_LOGIC;*

*Q: out STD\_LOGIC;*

*nQ: out STD\_LOGIC*

*);*

*ends\_bistable;*

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entity trigger is*

*port (*

*Ft: in STD\_LOGIC;*

*C: in STD\_LOGIC;*

*R: in STD\_LOGIC;*

*S: in STD\_LOGIC;*

*Q: out STD\_LOGIC;*

*nQ: out STD\_LOGIC*

*);*

*end trigger;*

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*entity t is*

*generic(*

*delay:time:=130ns*

*);*

*port (*

*t: in STD\_LOGIC;*

*c: in STD\_LOGIC;*

*r: in STD\_LOGIC;*

*pQ: out STD\_LOGIC;*

*nQ: out STD\_LOGIC*

*);*

*end t;*

*architecture t of t is*

*begin*

*process(c,r)*

*variableq:integer:=0;*

*--variabler:integer:=0;*

*begin*

*if (c'event and c='0' and r='0') then*

*if (t='1') then q:=1-q;*

*end if;*

*end if;*

*if (r'event and r='1') then q:=0;*

*end if;*

*if (q=1) then pQ<='1' after delay;nQ<='0' after delay;*

*elsenQ<='1' after delay;pQ<='0' after delay;*

*end if;*

*end process;*

*end t;*

*library IEEE;*

*use IEEE.std\_logic\_1164.all;*

*architecture not3 of not3 is*

*begin*

*out1<=(not in1) after 30 ns;*

*out2<=(not in2) after 30 ns;*

*out3<=(not in3) after 30 ns;*

*-- <<enter your statements here>>*

*end not3;*

*architecture or2 of or2 is*

*begin*

*out1<=in1 or in2 after 30 ns;*

*-- <<enter your statements here>>*

*end or2;*

*architecture and3 of and3 is*

*begin*

*out1<= not ((in1 and in2) and in3) after 30 ns;*

*-- <<enter your statements here>>*

*end and3;*

*architectures\_comb of s\_comb is*

*component and3 is*

*port (in1:in STD\_LOGIC;in2:in STD\_LOGIC;in3:in STD\_LOGIC;out1:out STD\_LOGIC);*

*end component;*

*signal S1,S2:STD\_LOGIC;*

*begin*

*D1:and3 port map(nQ,C,FT,F1);*

*D2:and3 port map(Q,C,FT,F2);*

*--D3:not3 port map(S1,S2,S2,F1,F,F2);*

*end s\_comb;*

*architectures\_bistable of s\_bistable is*

*component and3 is*

*port (in1:in STD\_LOGIC;in2:in STD\_LOGIC;in3:in STD\_LOGIC;out1:out STD\_LOGIC);*

*end component;*

*signal S1,S2:STD\_LOGIC;*

*begin*

*--S2<=nQ;*

*D1:and3 port map(R,F1,S1,S2);*

*D2:and3 port map(S,F2,S2,S1);*

*Q<=S2;*

*nQ<=S1;*

*ends\_bistable;*

*architecture trigger of trigger is*

*component and3 is*

*port (in1:in STD\_LOGIC;in2:in STD\_LOGIC;in3:in STD\_LOGIC;out1:out STD\_LOGIC);*

*end component;*

*components\_bistable is*

*port (R:in STD\_LOGIC;F1:in STD\_LOGIC;F2:in STD\_LOGIC;S:inSTD\_LOGIC;Q:outSTD\_LOGIC;nQ:out STD\_LOGIC);*

*end component;*

*components\_comb is*

*port (Q:inSTD\_LOGIC;FT:inSTD\_LOGIC;C:inSTD\_LOGIC;nQ: in STD\_LOGIC;F1:out STD\_LOGIC;F2:out STD\_LOGIC);*

*end component;*

*signal S1,S2,S3,S4,S5,S6,S7,S8,S9:STD\_LOGIC;*

*begin*

*D1:s\_comb port map(S8,FT,C,S9,S1,S2);*

*D2:s\_bistable port map(R,S1,S2,S,S4,S5);*

*D3:and3 port map(C,C,C,S3);*

*D4:and3 port map(S4,S4,S3,S6);*

*D5:and3 port map(S5,S3,S3,S7);*

*D6:s\_bistable port map(R,S6,S7,S,S8,S9);*

*Q<=S8;*

*nQ<=S9;*

*end trigger;*